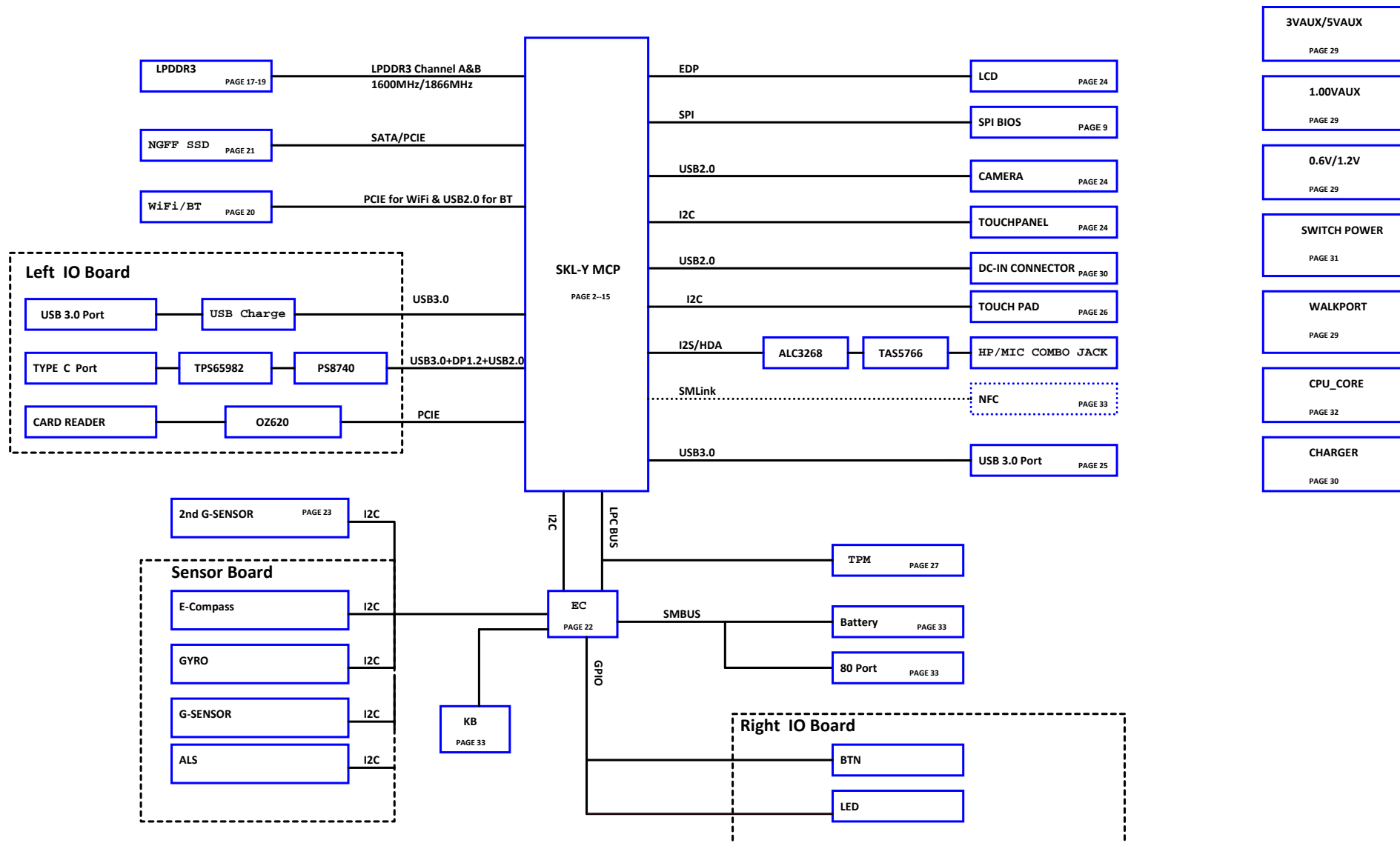
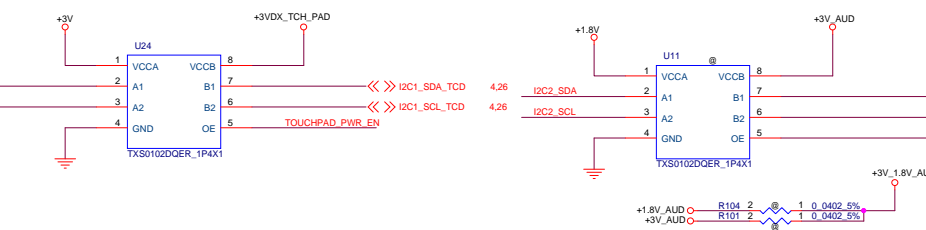
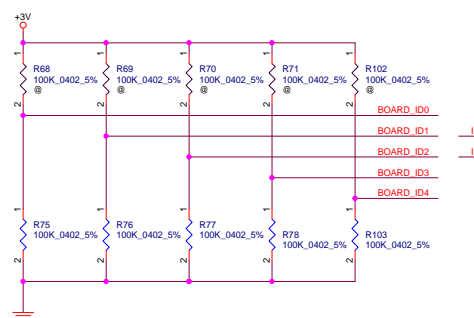
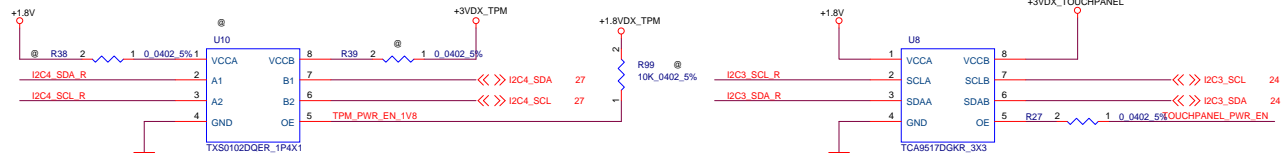
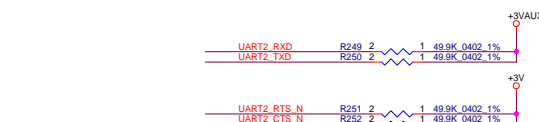
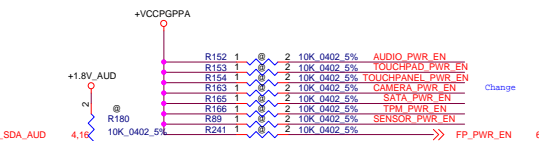
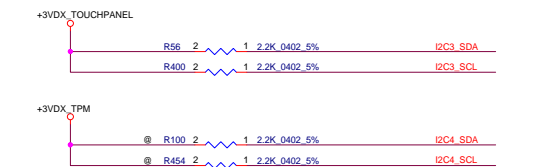
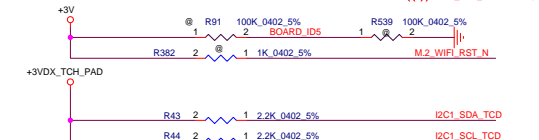
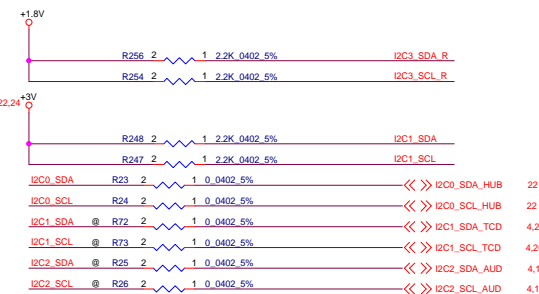


Maksim 12.5 SKL-Y CS SDV Schematic Block Diagram




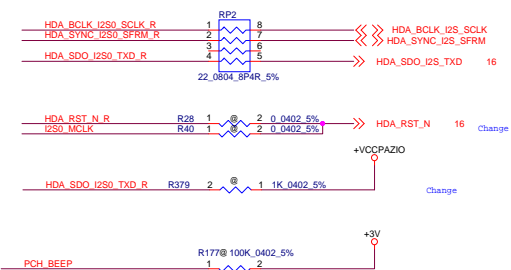
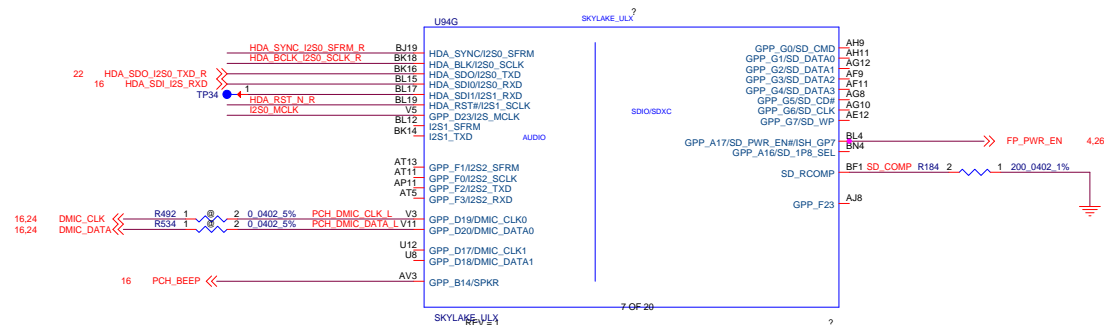


BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0	Description	SRU
1	0	0	1	0	Elpida LPDDR3 8GB 1866	1
1	0	0	0	0	Samsung LPDDR3 8GB 1866	2
1	1	1	1	0	Hynix LPDDR3 4GB 1866	3

BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0	Description	
1	0	0	0	0	Samsung LPDDR3 8GB 1866	
1	1	0	0	0	Hynix LPDDR3 8GB 1866	
1	0	0	1	0	Elpida LPDDR3 8GB 1866	
1	1	1	1	0	Hynix LPDDR3 4GB 1866	
1	1	0	1	0	Samsung LPDDR3 4GB 1866	
1	0	1	1	0	Elpida LPDDR3 4GB 1866	

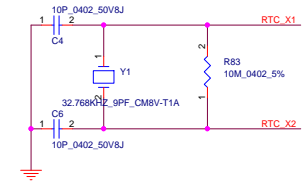
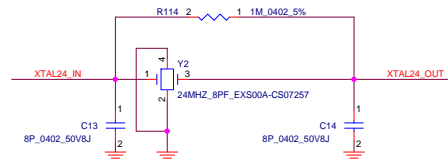
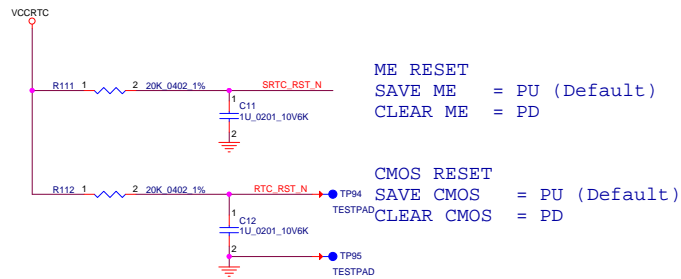
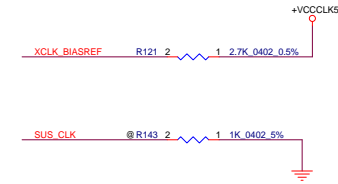
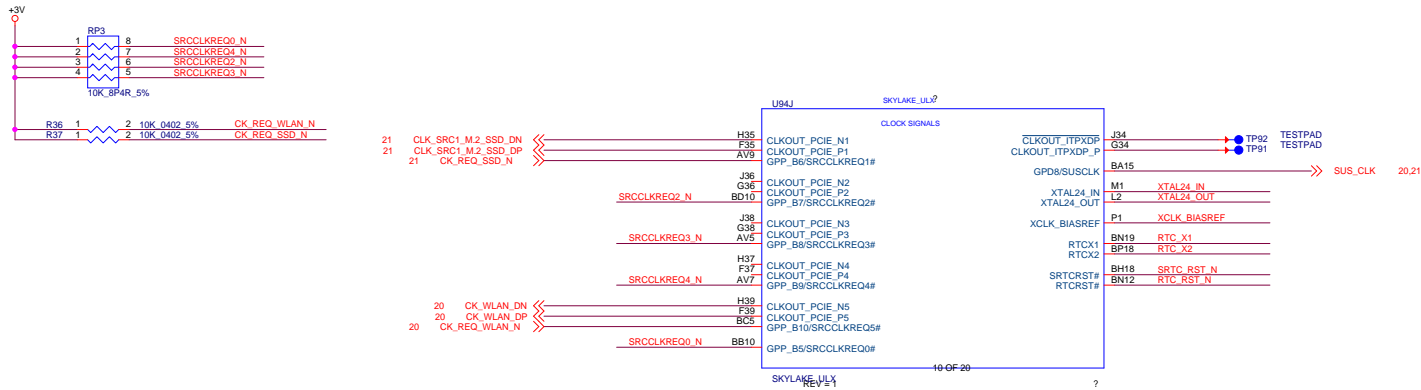
GSPI1_MOSI / GPP_B22
 Boot BIOS Strap_Bit_BBS
 Rising edge of PCH_PWROK
 This Signal has a weak internal pull-down.
 This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).
 0 SPI (Default)
 1 LPC
 Notes:
 1. The internal pull-down is disabled after PLTRST# deasserts.
 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.
 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.
 4. This signal is in the primary well.

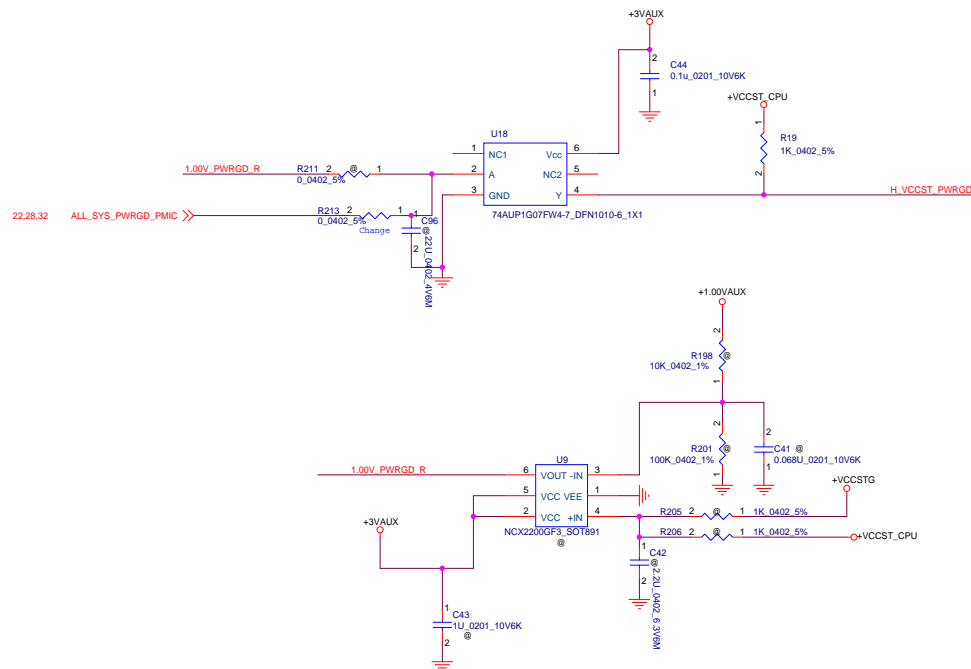
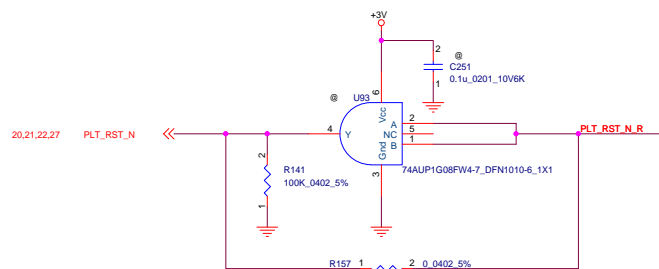
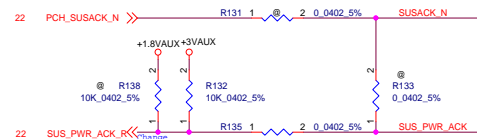
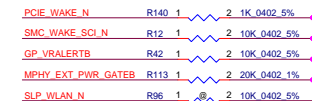
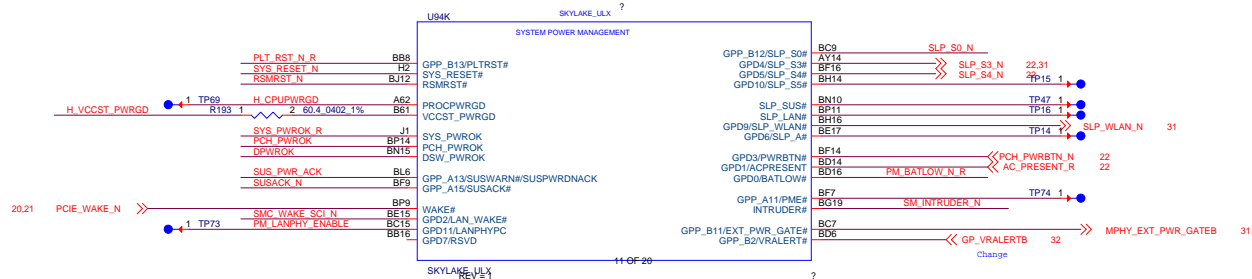
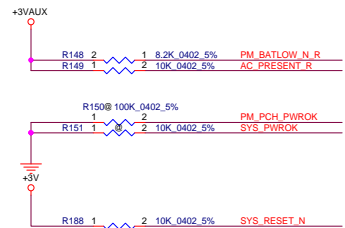
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Title SKL MCP (GPIO)			
Size C	Document Number	Rev v1.0	
	Maksim		
Date: Monday, November 02, 2015		Sheet 4 of 37	
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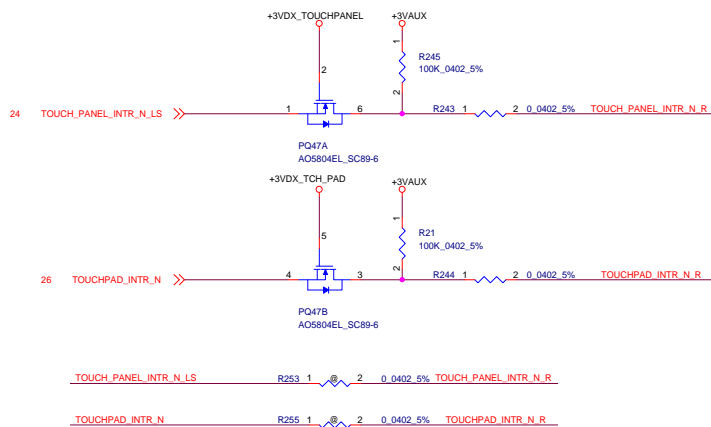
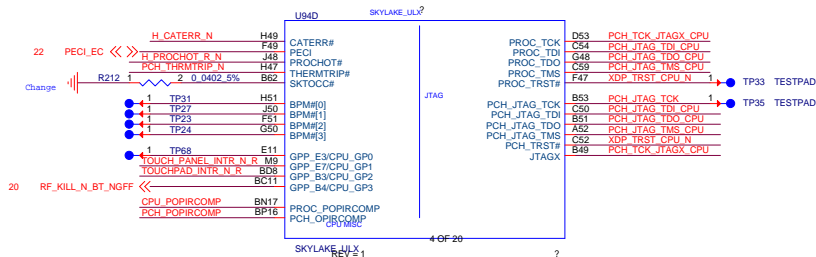
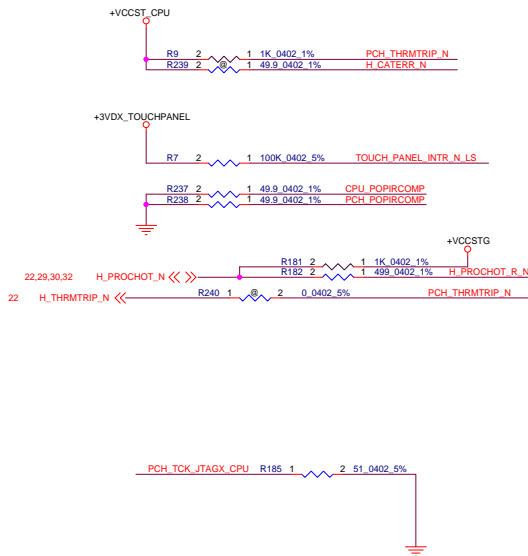


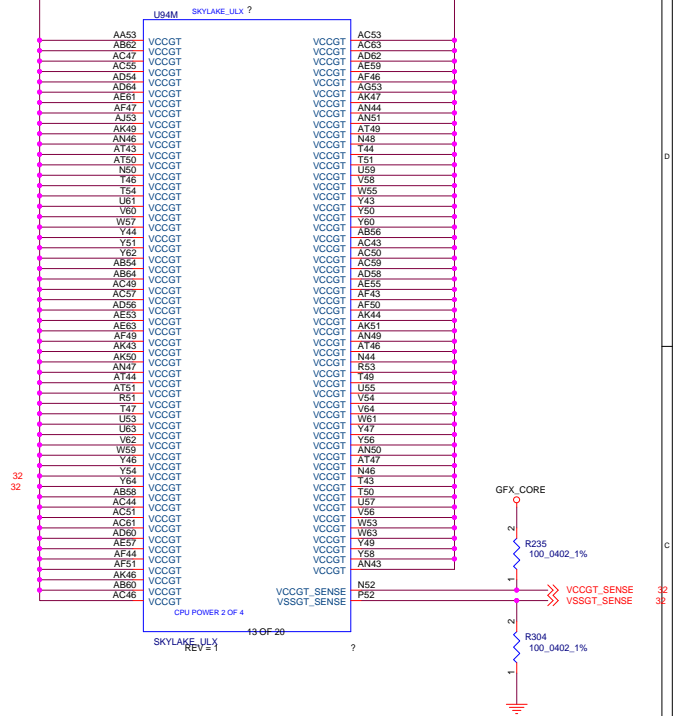
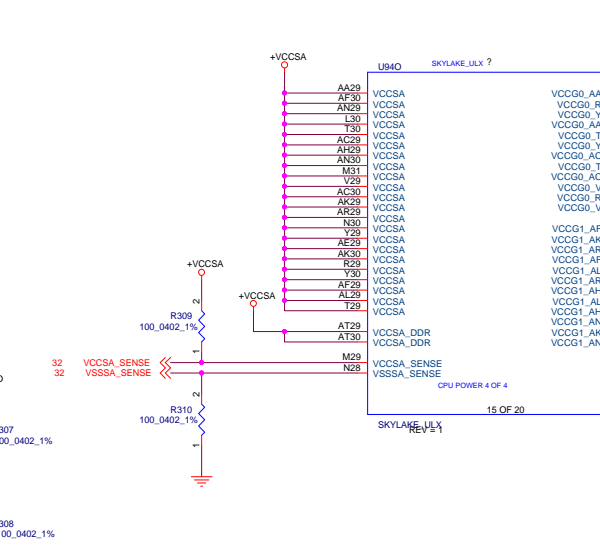
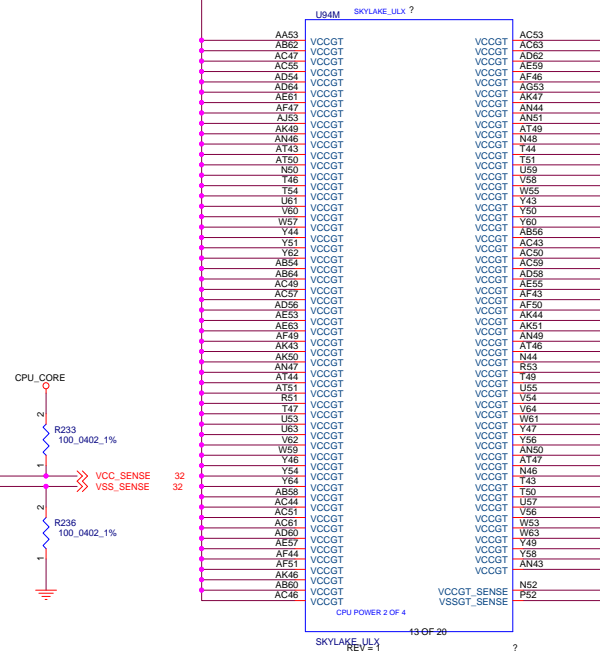
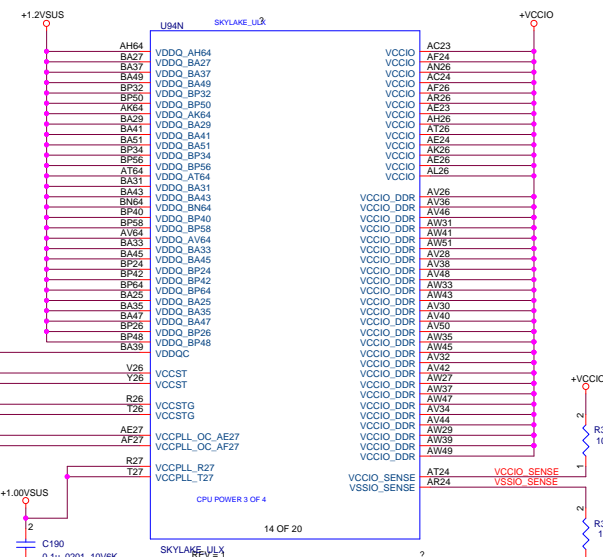
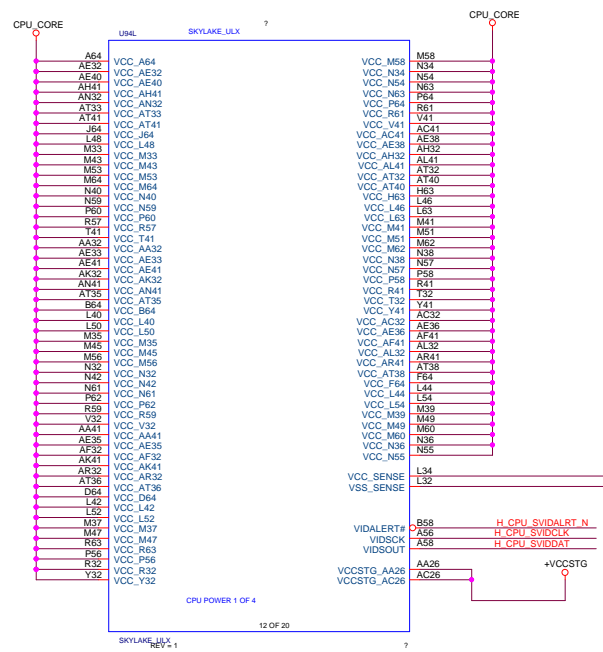
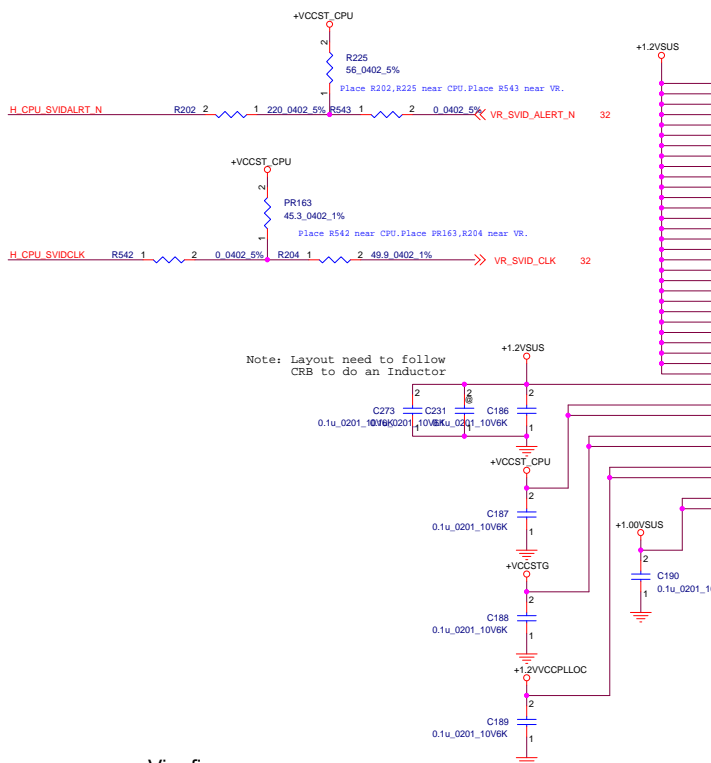
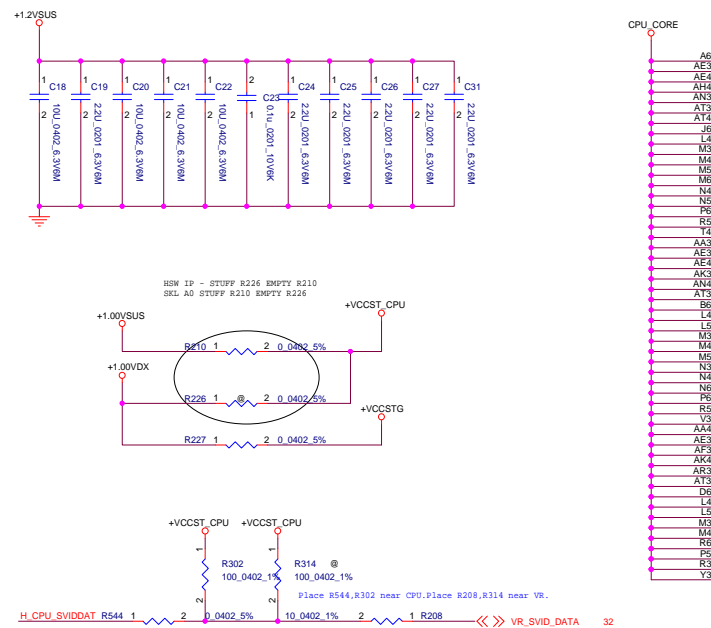
HDA_SDO_I2S0_TXD0
Flash Descriptor Security Override
Rising edge of PCH_PWROK
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
Notes:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
3. This signal is in the primary well.

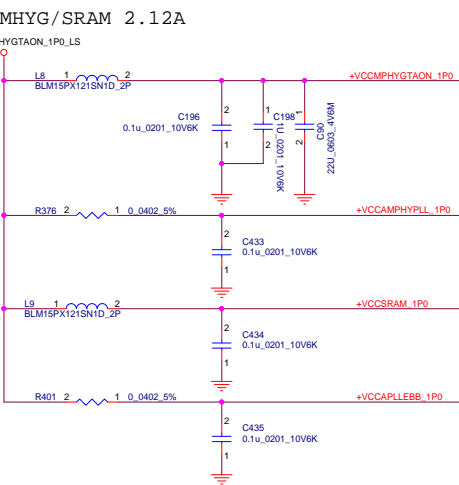
SPKR / GPP_B14 Top Swap Override
Rising edge of PCH_PWROK
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FW or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.
Notes:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. Software will not be able to clear the Top Swap bit until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4).
4. This signal is in the primary well.



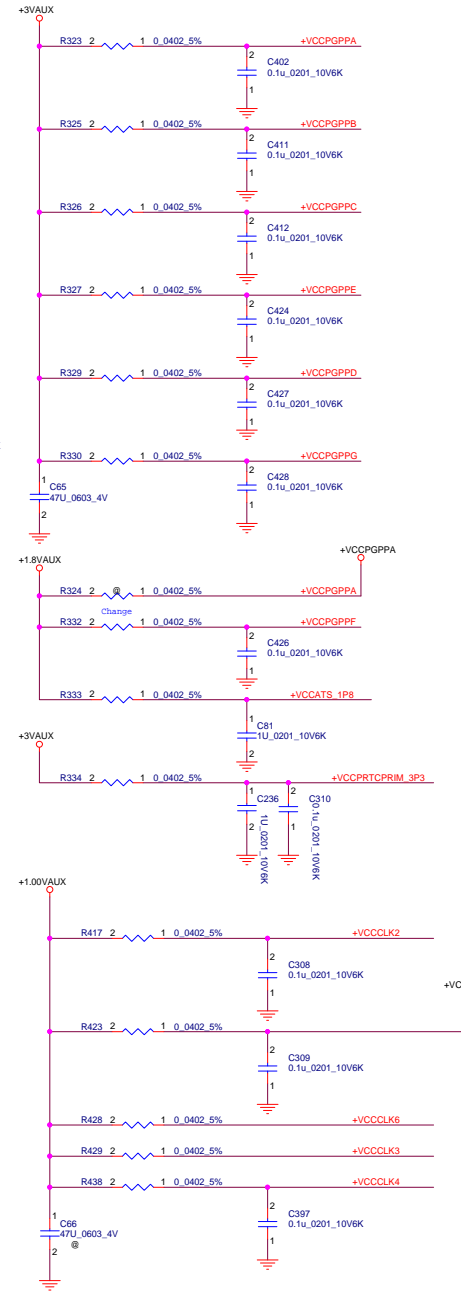
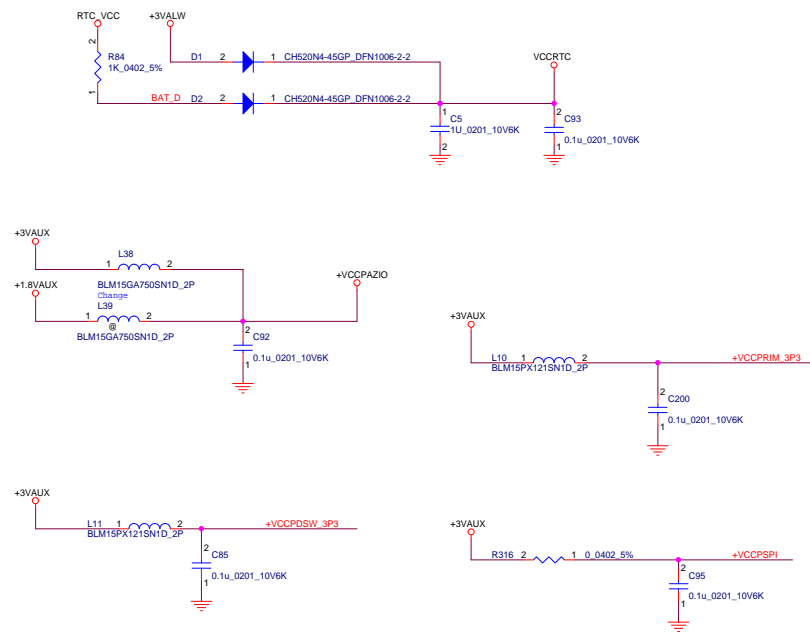
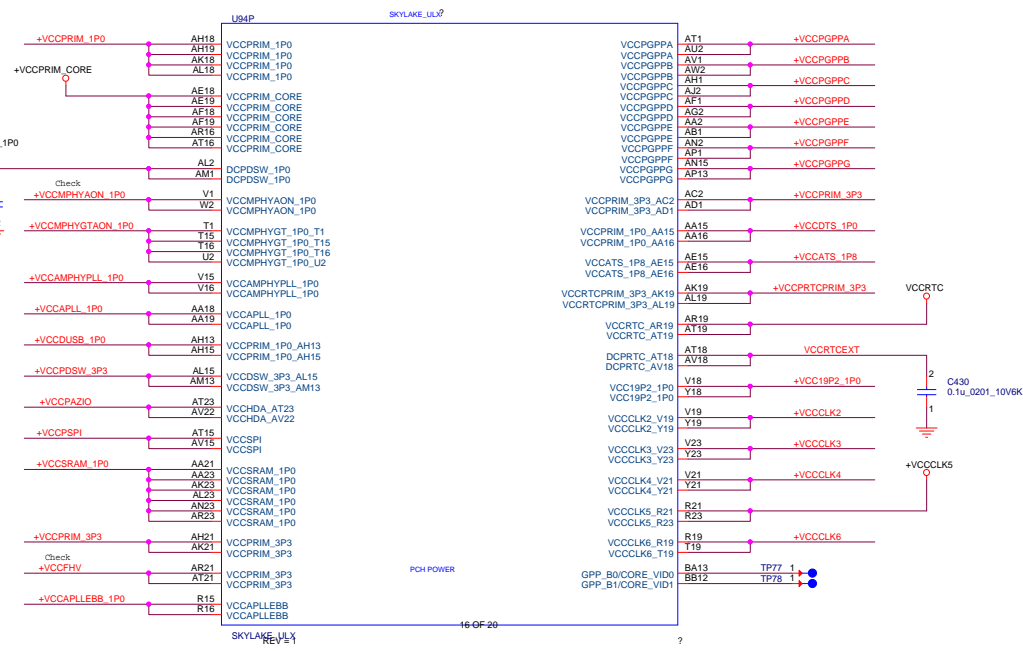


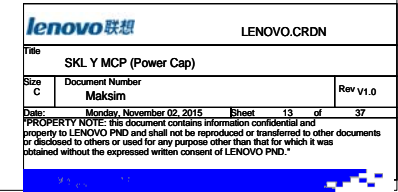


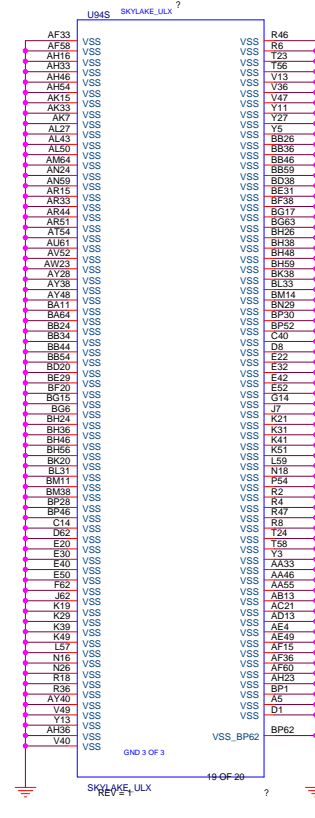
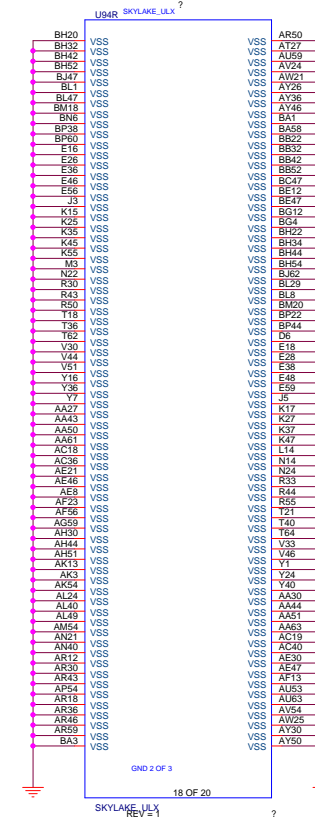
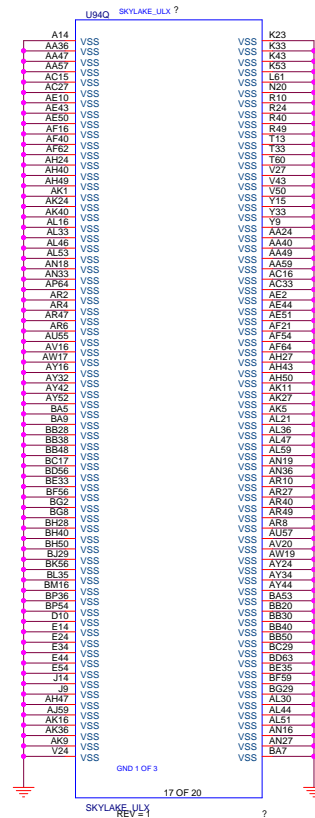


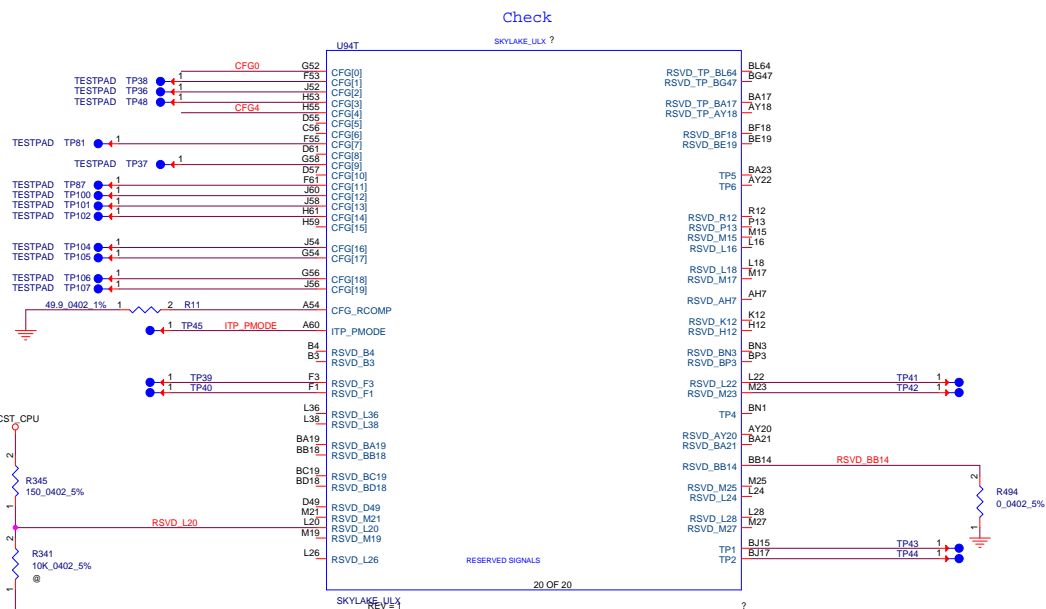


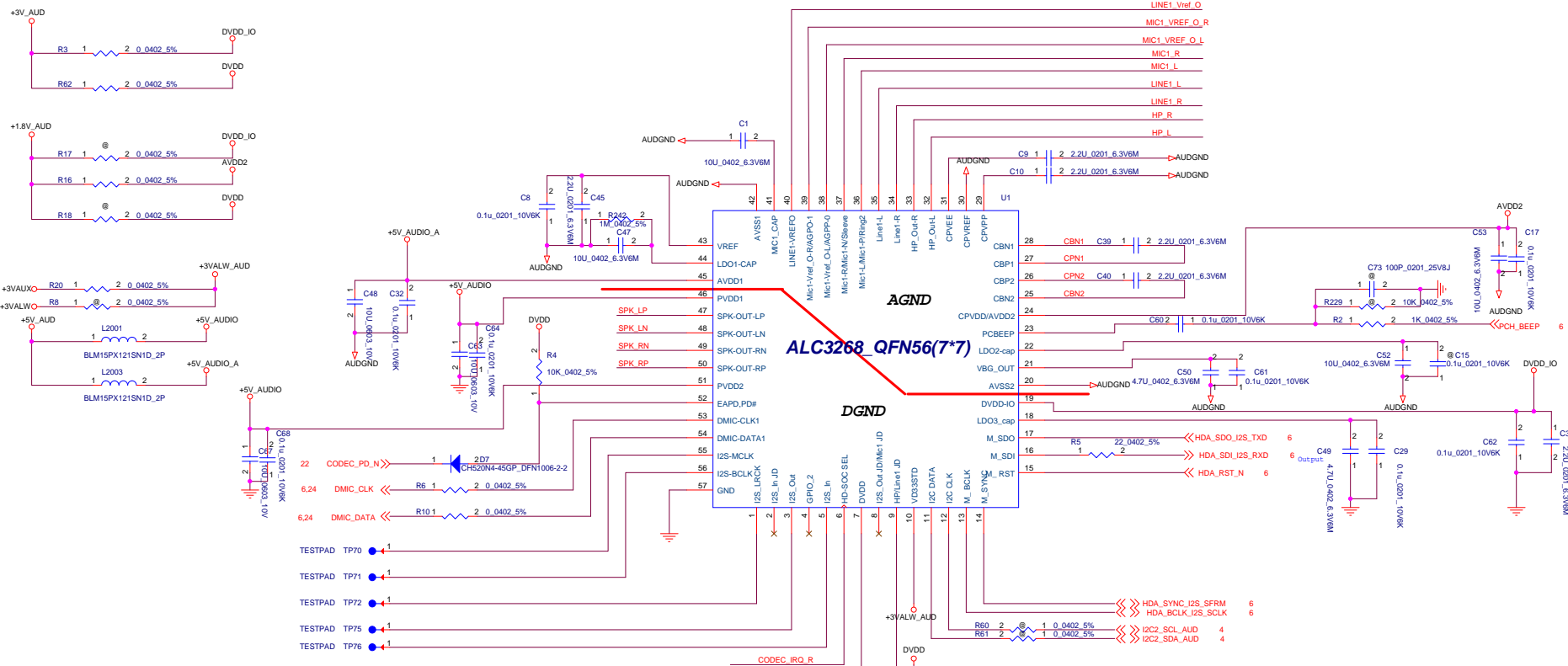
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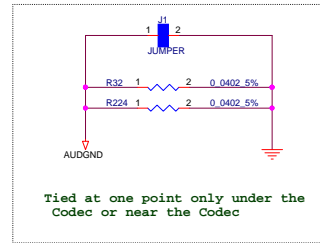
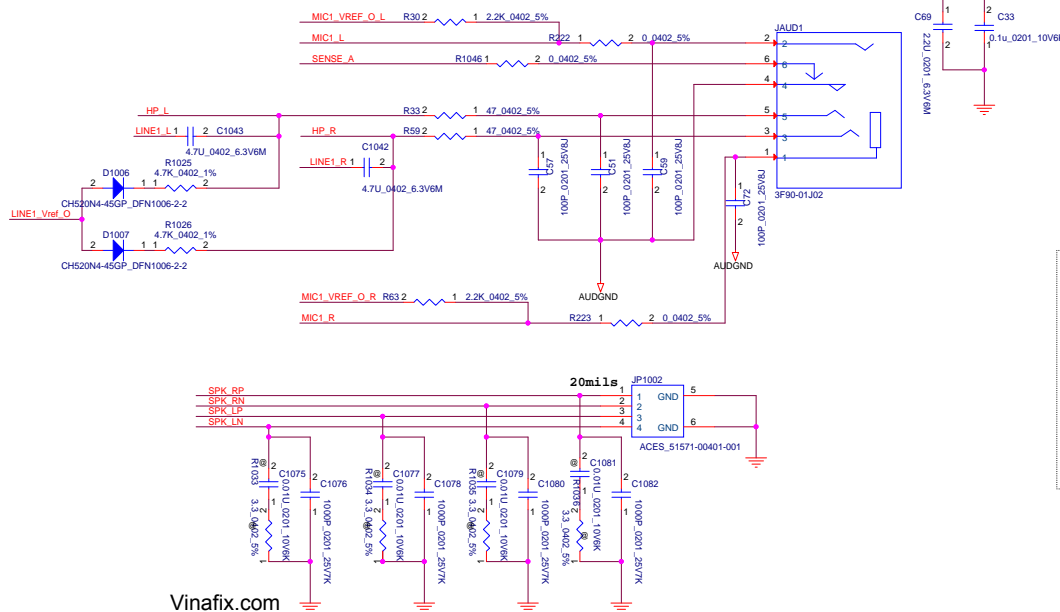








global headset normal open



PIN6 is for HDA and I2S strap pin.
High is HDA enable. (Default)
Low is I2S enable.

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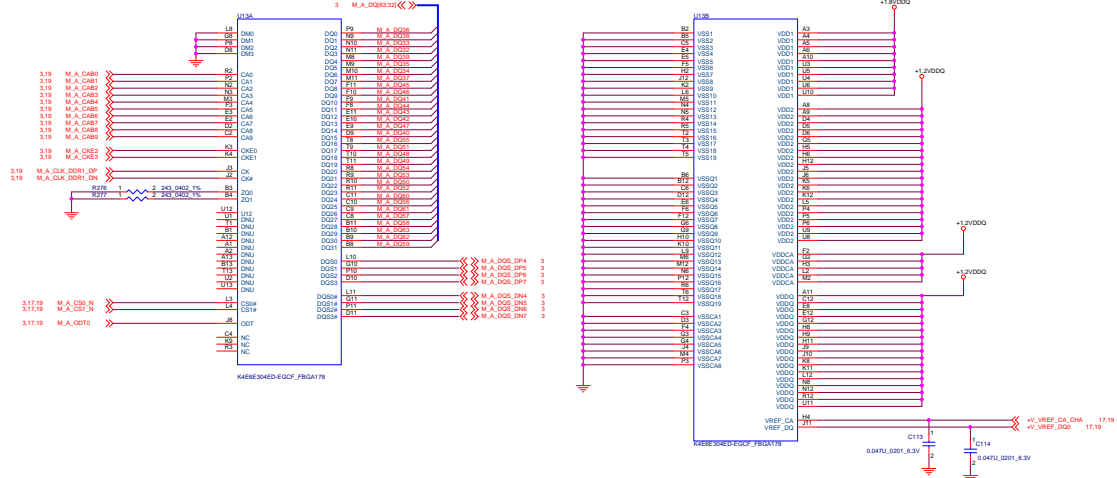
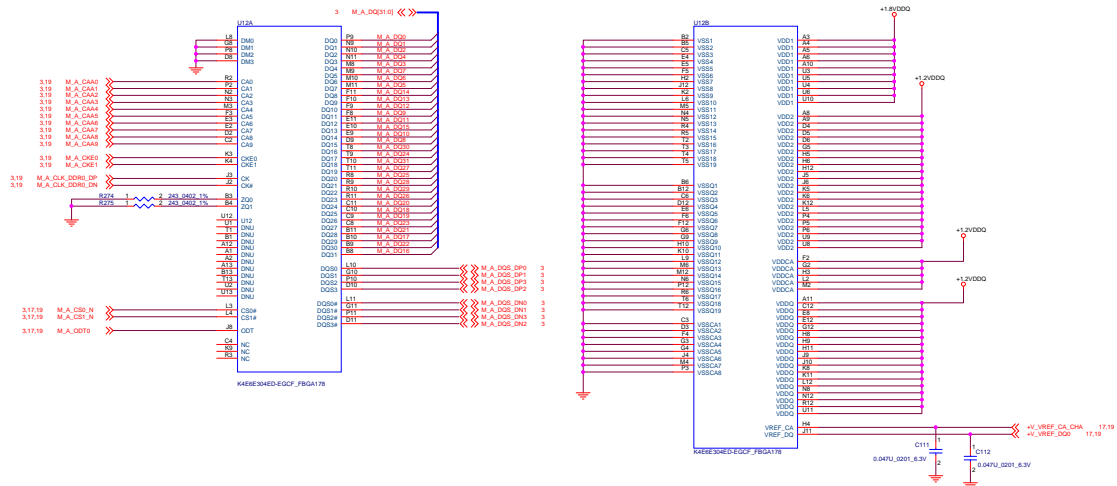
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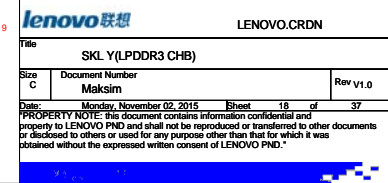
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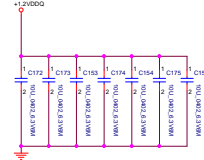
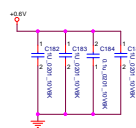
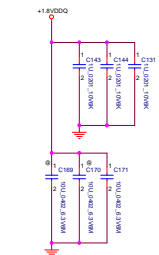
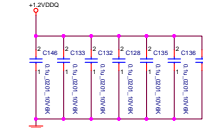
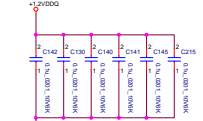
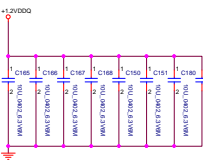
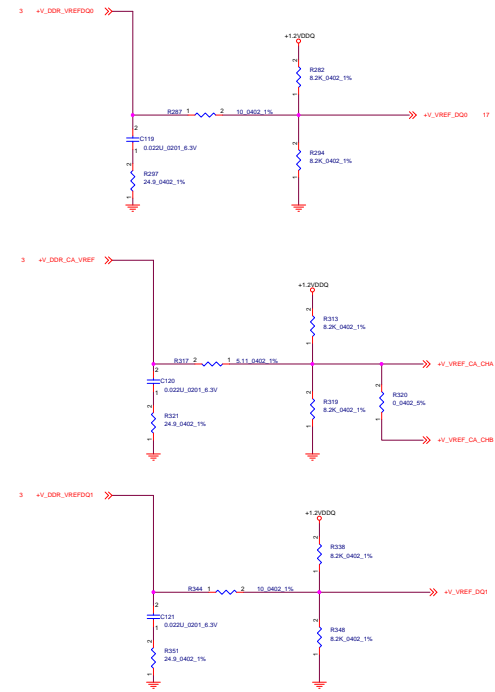
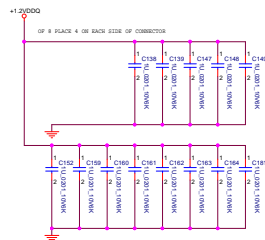
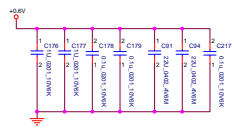
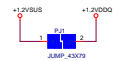
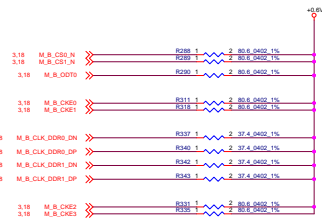
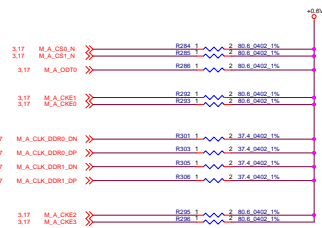
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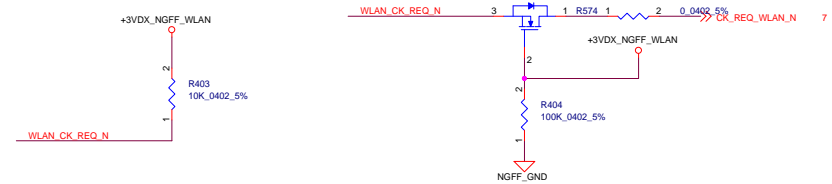
Rev V1.0

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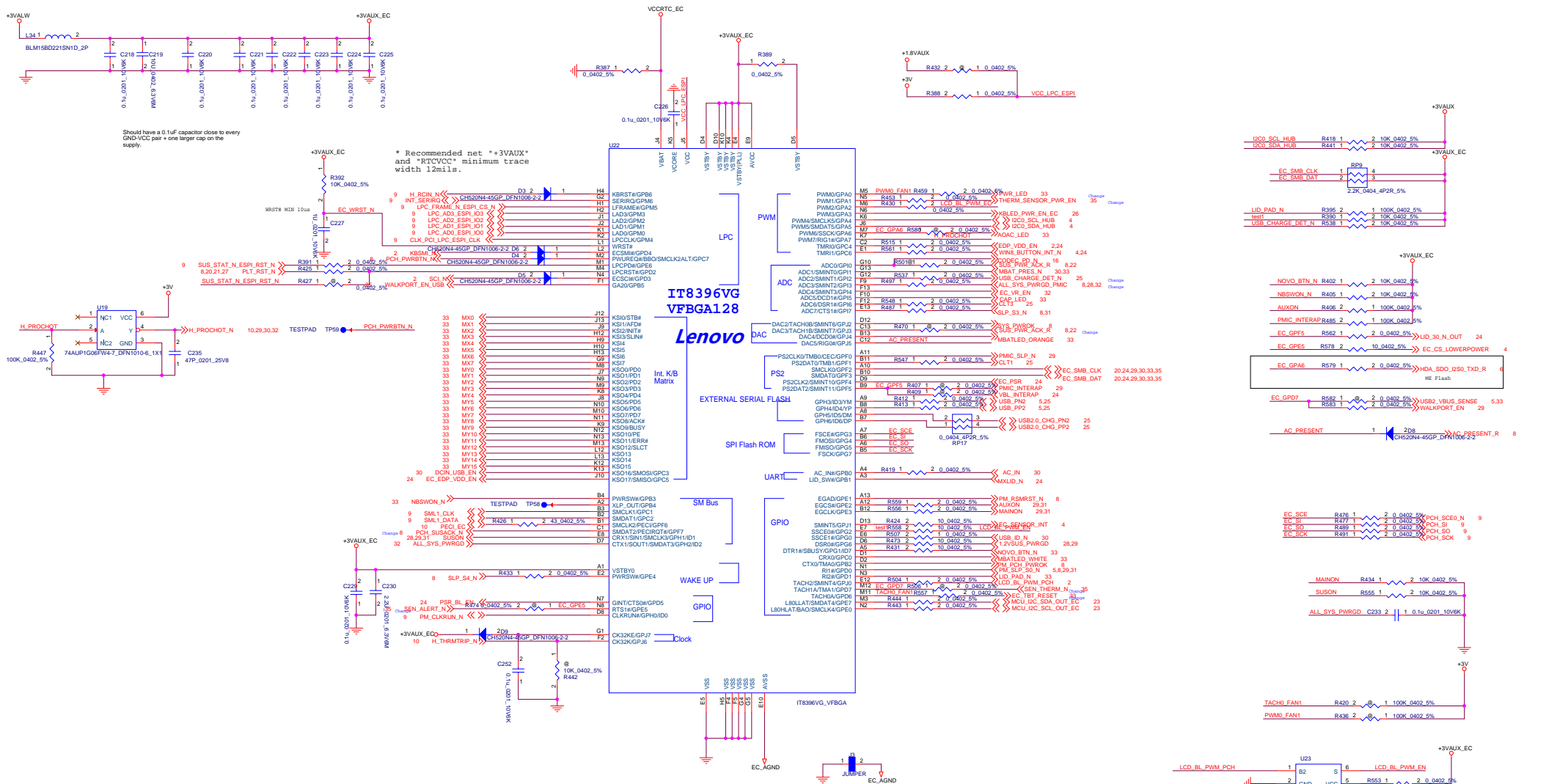








[illegible]

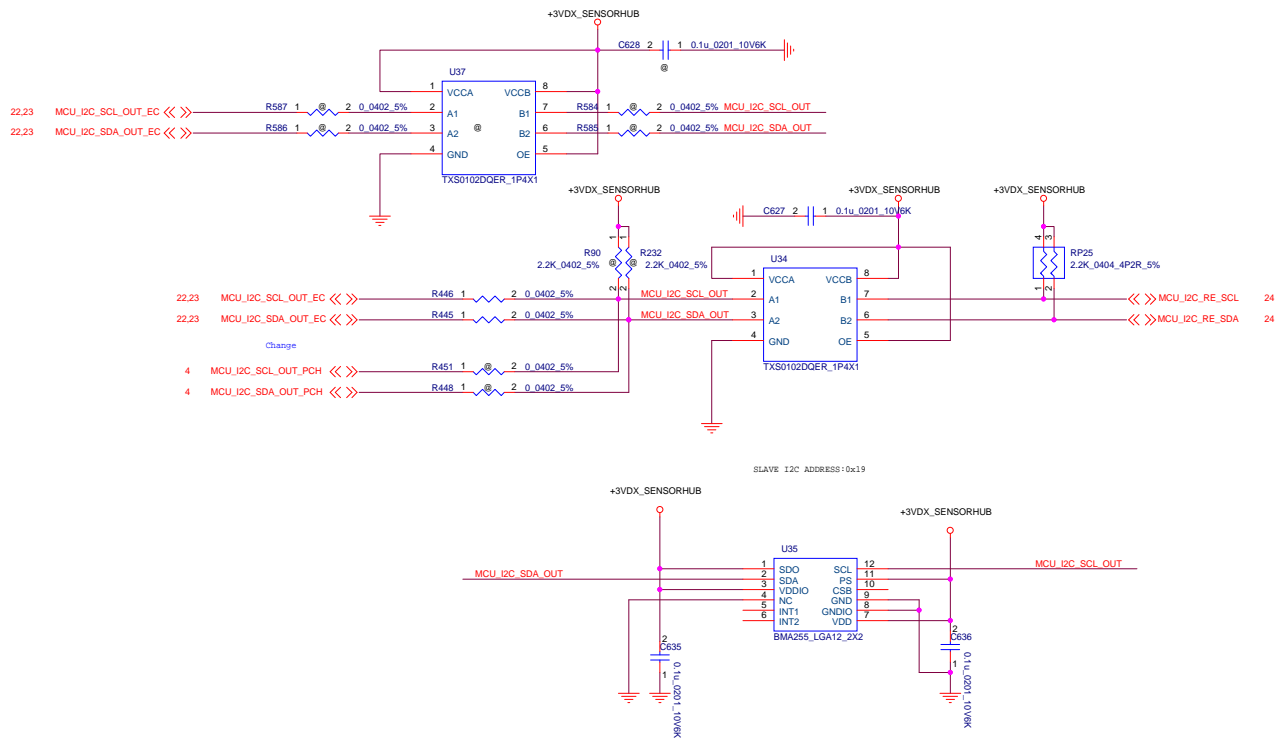


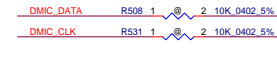
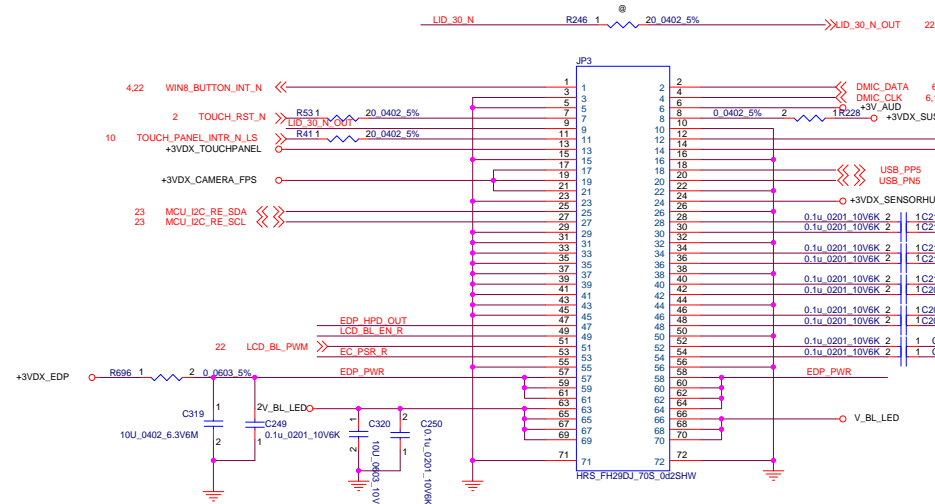
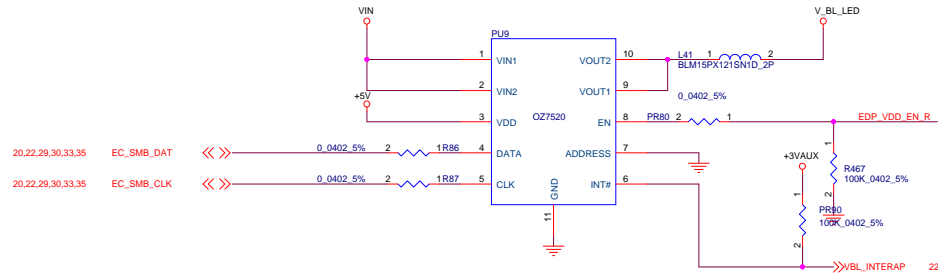
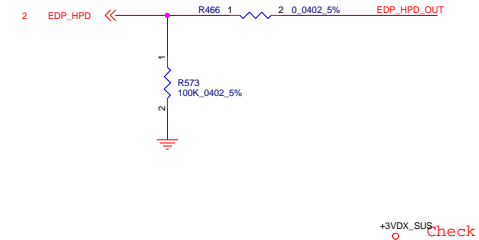
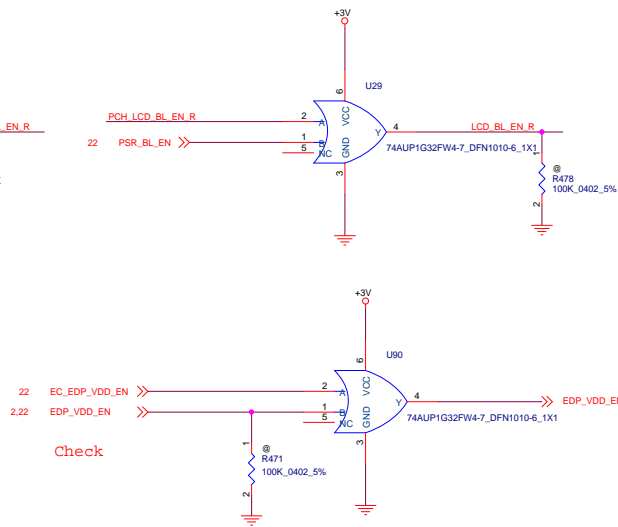
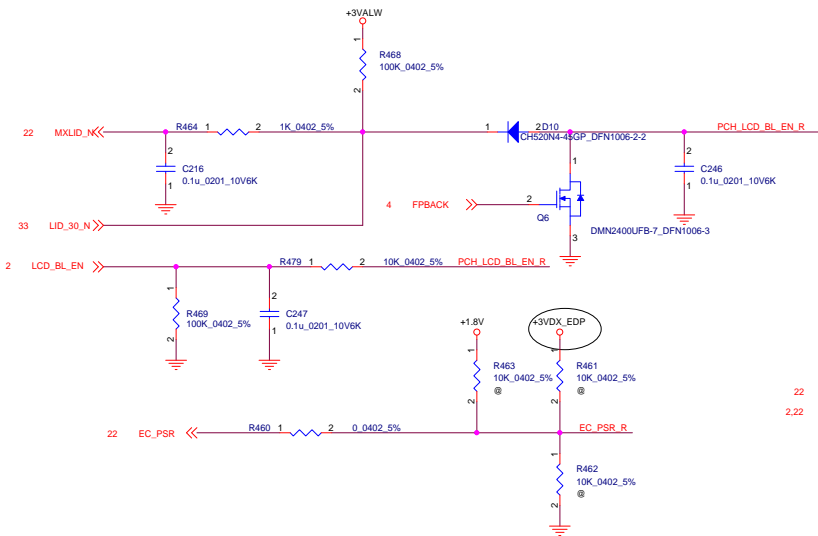
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:

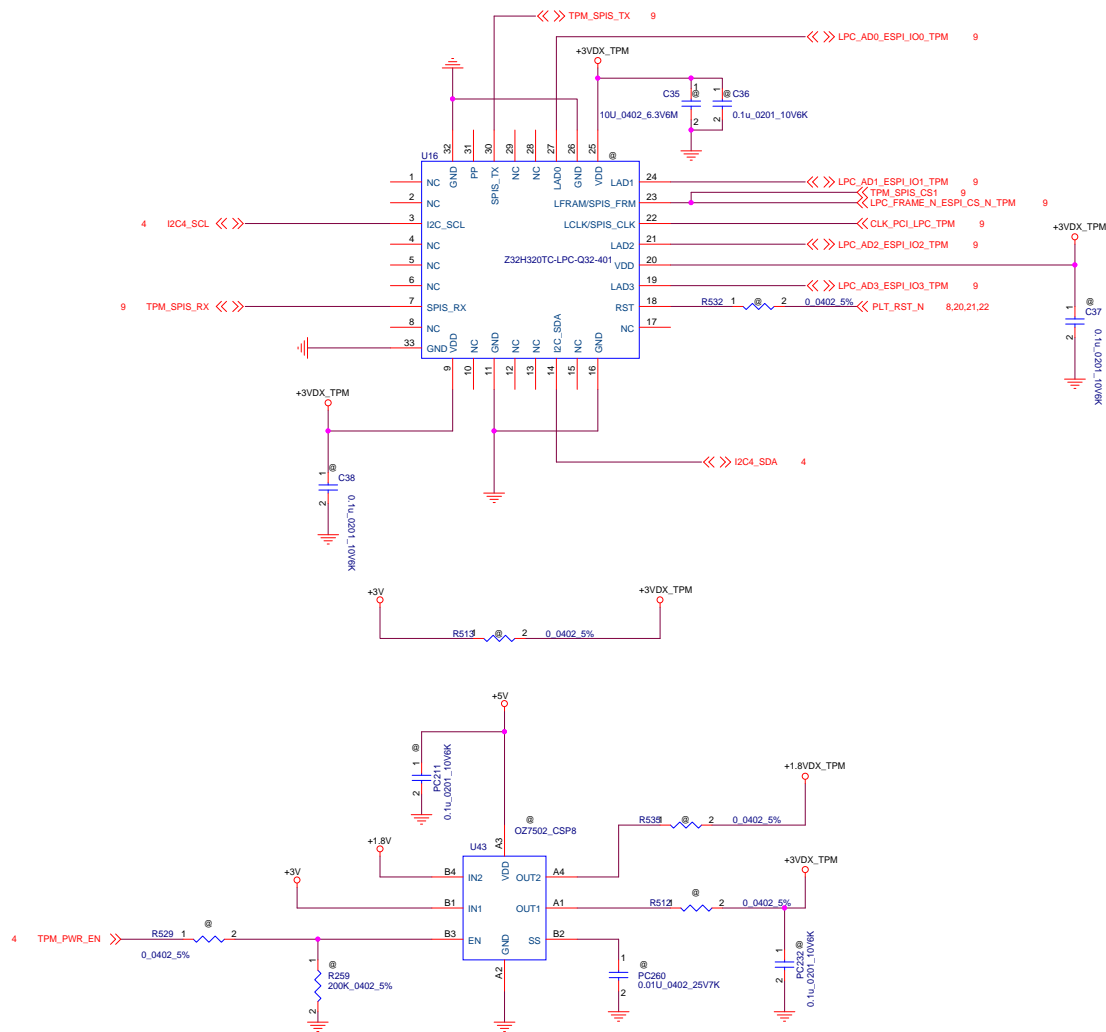
- (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
- (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

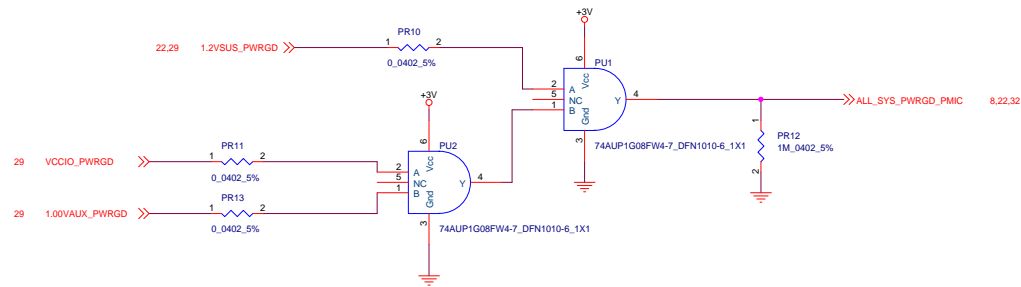
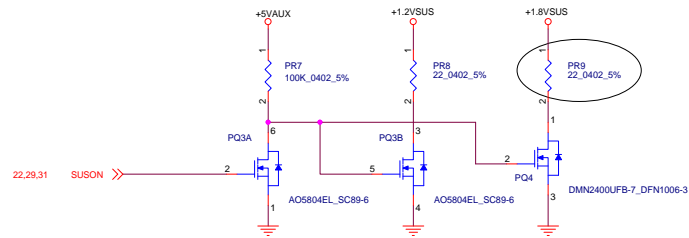
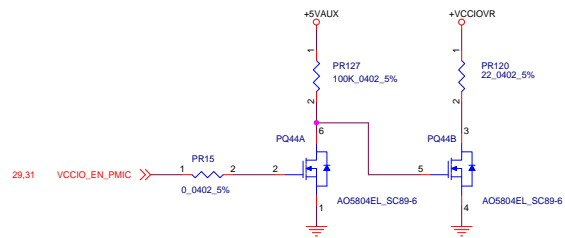
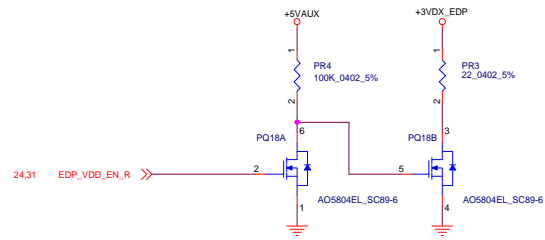
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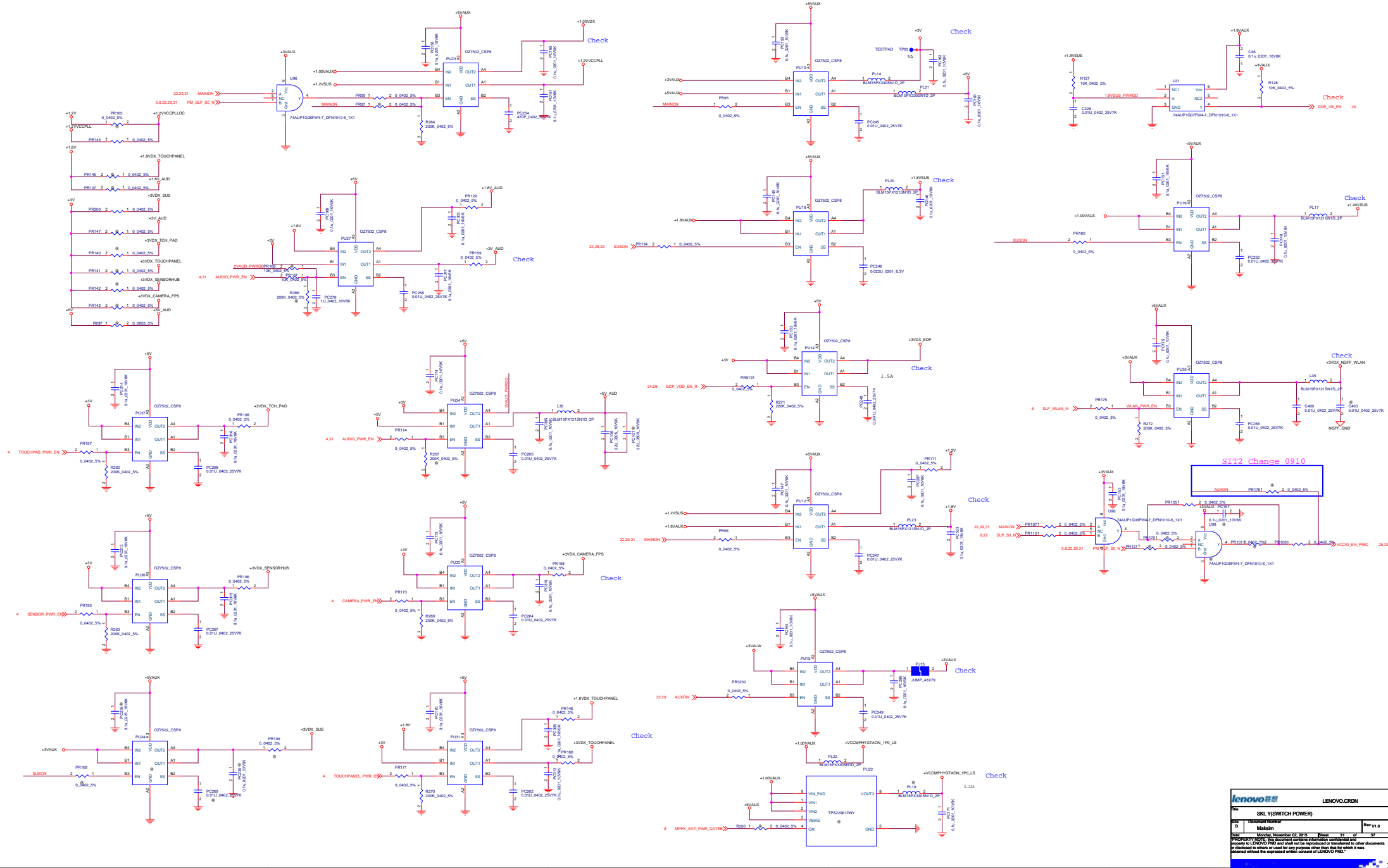
- (1) Each input pin should be driven or pulled.
- (2) Each output-drain output pin should be pulled.



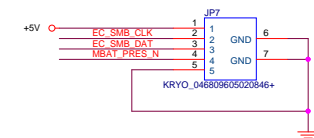
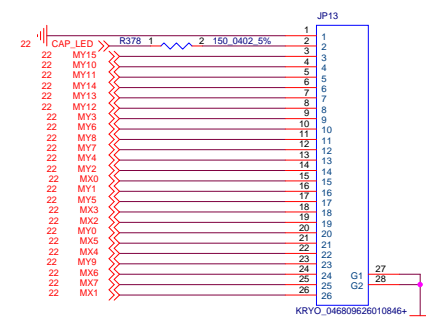
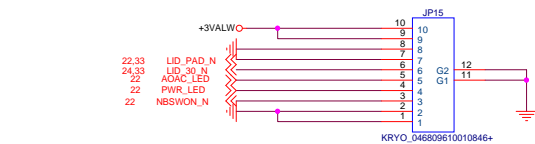






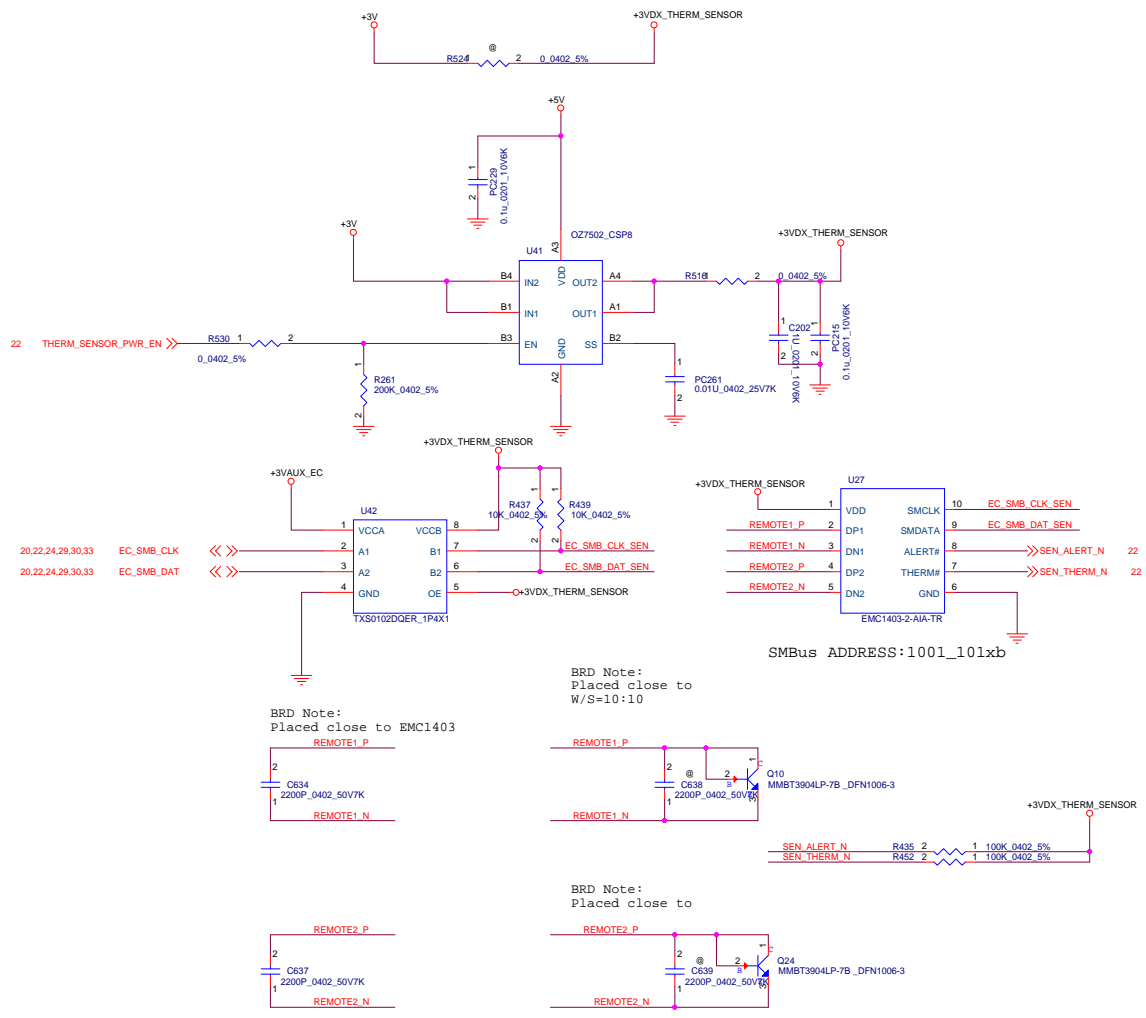


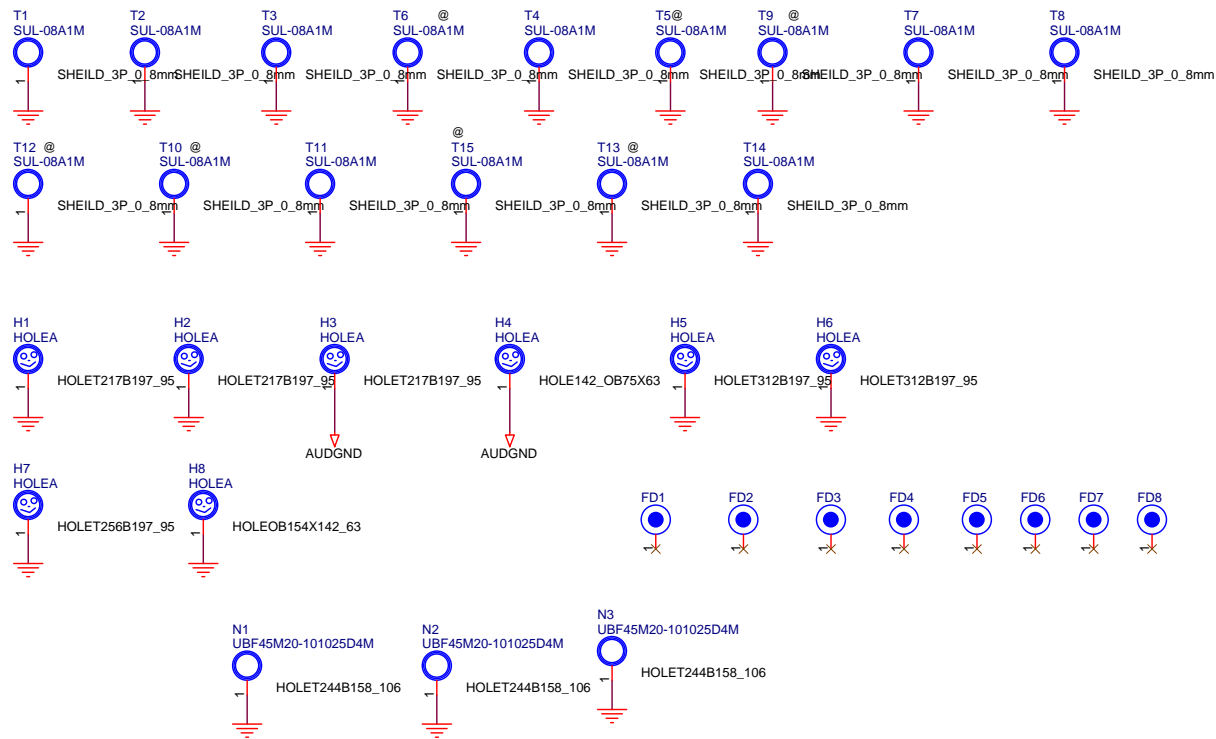


lenovo		LENOVO ORDIN	
Rev	1.0	Rev	1.0
Model	Y530	Model	Y530
Part	SKL Y530 (POWER)	Part	SKL Y530 (POWER)
Rev	1.0	Rev	1.0
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Title			
SKL Y (AMP)			
Size	Document Number		Rev
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Date:	Monday, November 02, 2015	Sheet 34 of	37
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Title			
SKL Y(MOUNTING HOLE/EMI)			
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